What is Claimed is:

1. A digital system comprising a microprocessor having an instruction execution pipeline with a plurality of pipeline phases, wherein the microprocessor comprises:

program fetch circuitry operable to perform a first portion of the plurality of pipeline phases;

instruction decode circuitry connected to receive fetched instructions from the program fetch circuitry, the instruction decode circuitry operable to perform a second portion of the plurality of pipeline phases; and

at least a first functional unit connected to receive control signals from the instruction decode circuitry, the functional unit operable to perform a third portion of the plurality of pipeline phases, the third portion being execution phases, wherein the first functional unit comprises:

byte intermingling circuitry connected to receive a first source operand and a second source operand and having outputs connected to provide a destination operand in response to the control signals, wherein the byte intermingling circuitry is operable to treat the first and second operands each as a number N1 of ordered fields, such that the destination operand consists of a number N2 of fields selected from the N1 fields of the first source operand intermingled with a number N3 of fields selected from the N1 fields of the second source operand; and

wherein the first functional unit is operable to provide the destination operand intermingled in accordance to each of a set of byte intermingling instructions.

2. The digital system of Claim 1, wherein the byte intermingling circuitry is operable to receive the first source operand and second operand

and to provide the destination operand during a single pipeline execution phase.

3. The digital system of Claim 1, wherein the byte intermingling circuitry is operable to provide a destination operand that consists of a N1-1 fields selected from the second operand and one field selected from the first source operand.

4. The digital system of Claim 3, wherein the byte intermingling circuitry is operable the select a first N1-1 fields from a most significant portion of the second operand and to select a first field from a least significant portion of the first operand, such that the first field from the first operand is placed in a most significant portion of the destination operand, whereby a shift right and byte merge operation is performed.

5. The digital system of Claim 4, wherein the byte intermingling circuitry is operable the select a second N1-1 fields from a least significant portion of the second operand and to select a second field from a most significant portion of the first operand, such that the second field from the first operand is placed in a least significant portion of the destination operand, whereby a shift left and byte merge operation is performed.

6. The digital system of Claim 1, wherein the byte intermingling circuitry is operable to provide the destination operand by placing a most significant set of the N1 fields selected from the second operand in a most significant portion of the destination operand and by placing a least significant set of the N1 fields selected from the second operand in a most significant portion of the destination, whereby a byte swap operation is performed.

7. The digital system of Claim 6, wherein the byte intermingling circuitry is operable to operable to provide the destination operand by placing a least significant set of the N1 fields selected from the second operand in a least significant portion of the destination operand and by placing a least significant set of the N1 fields selected from the second operand in a most significant portion of the destination, whereby a byte pack operation is performed.

8. The digital system of Claim 6, wherein the byte intermingling circuitry is operable to operable to provide the destination operand by placing a least significant one of the N1 fields selected from the second operand in a least significant portion of the destination operand and by placing a next to least significant one the N1 fields selected from the second operand in a most significant portion of the destination, whereby a byte unpack operation is performed.

9. The digital system of Claim 1, further comprising a register file connected to the first functional unit for providing the first and second source operands and connected to the first functional unit to receive the destination operand.

10. The digital system of Claim 1, wherein each of the set of byte intermingling instructions has a field for identifying a predicate register.

11. The digital system of Claim 1 being a cellular telephone, further comprising:

an integrated keyboard connected to the CPU via a keyboard adapter;

a display, connected to the CPU via a display adapter;

radio frequency (RF) circuitry connected to the CPU; and

an aerial connected to the RF circuitry.

12. A method of operating a digital system having a microprocessor a set of byte intermingling instruction, comprising the steps of:

fetching a first type of byte intermingling instruction for execution;

fetching a first source operand and a second operand selected by the first type of byte intermingling instruction;

treating the first and second source operands as a set of N1 fields;

intermingling selected ones of the N1 fields from the first operand and selected ones of the N1 fields from the second operand in a first selected order in accordance with the first type of byte intermingling instruction to form a first type of intermingled fields; and

writing a destination operand with the first type of intermingled fields.

13. The method of Claim 12, further comprising the steps of:

fetching a second type of byte intermingling instruction for execution;

fetching a first source operand and a second operand selected by the second type of byte intermingling instruction;

treating the first and second source operands as a set of N1 fields;

intermingling selected ones of the N1 fields from the first operand and selected ones of the N1 fields from the second operand in a second selected order in accordance with the second type byte intermingling instruction to form a second type of intermingled fields; and

writing a destination operand with the second type of intermingled fields.

14. The method of Claim 11, wherein the step of intermingling is performed during a single execution phase of the microprocessor.